Artificial Intelligence Processor

- AB9, Complying with ISO26262 -

2019.10.10

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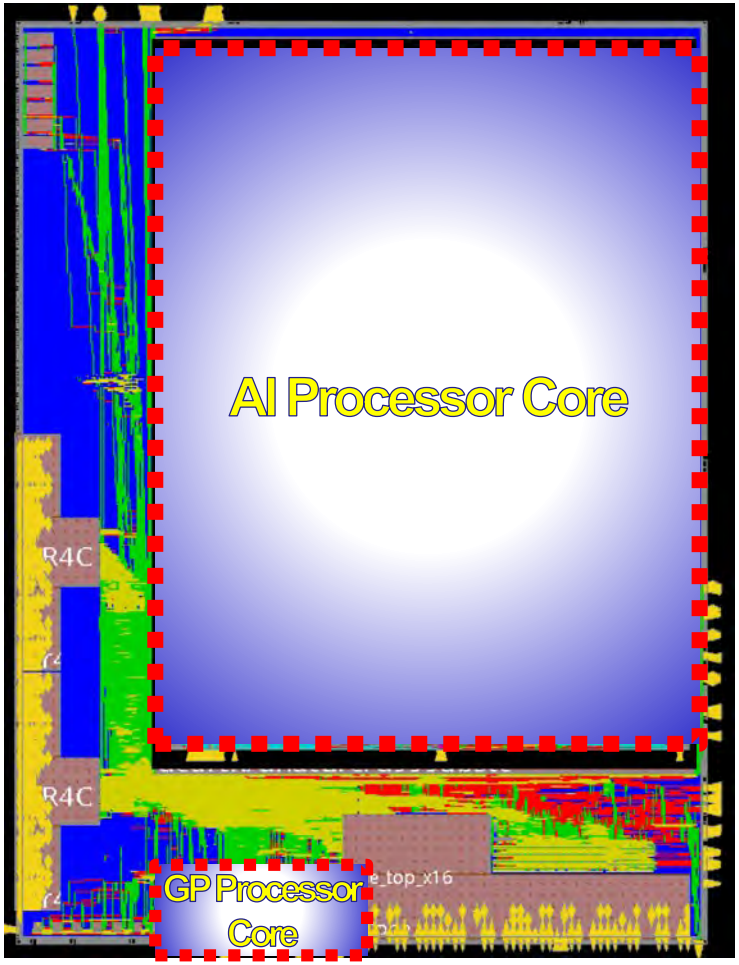
Content

AI Processor

국내최초 32TFLOPS AI 프로세서 독보적 설계기술 및 반도체 보유

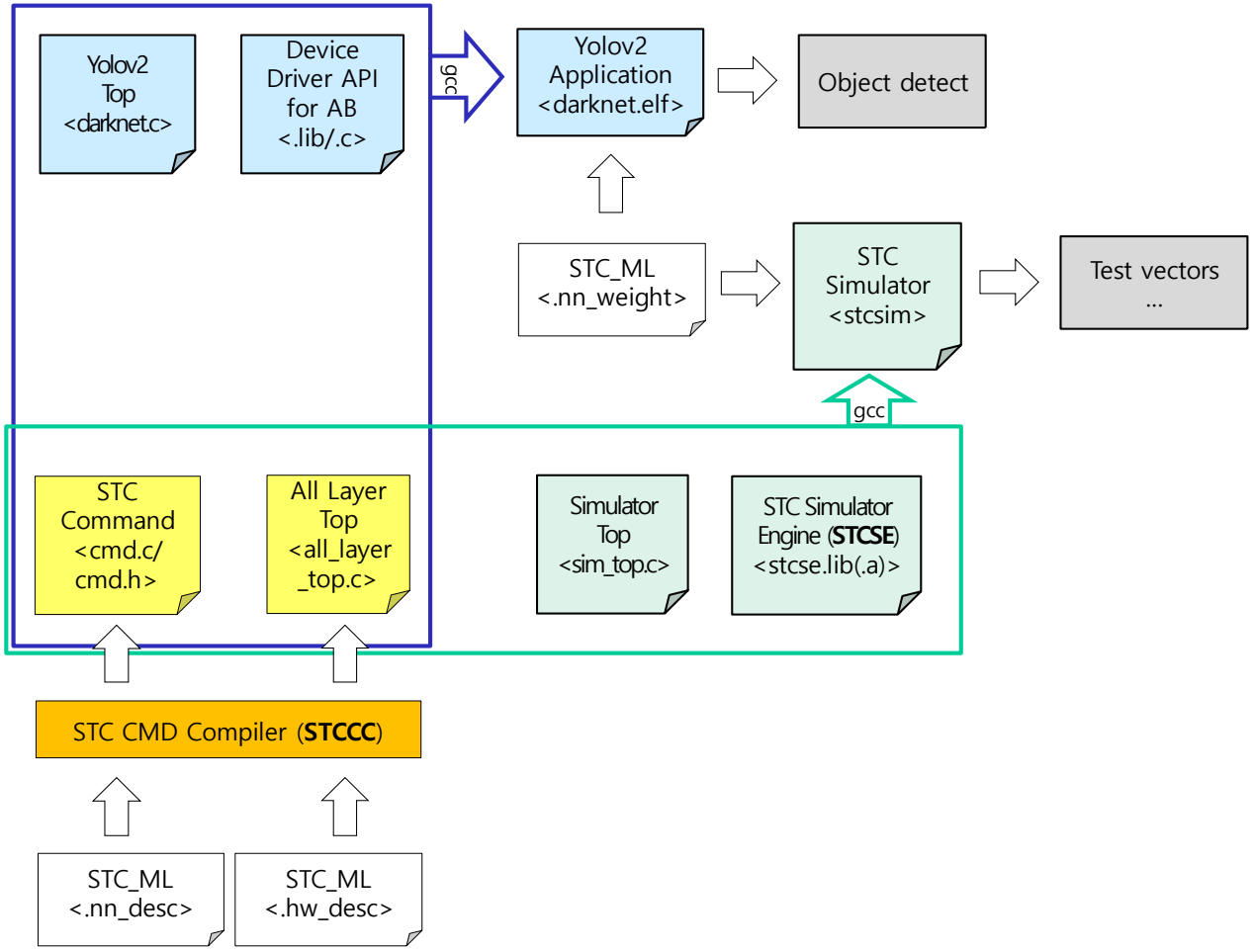


AB9, 494mm^2@28nm

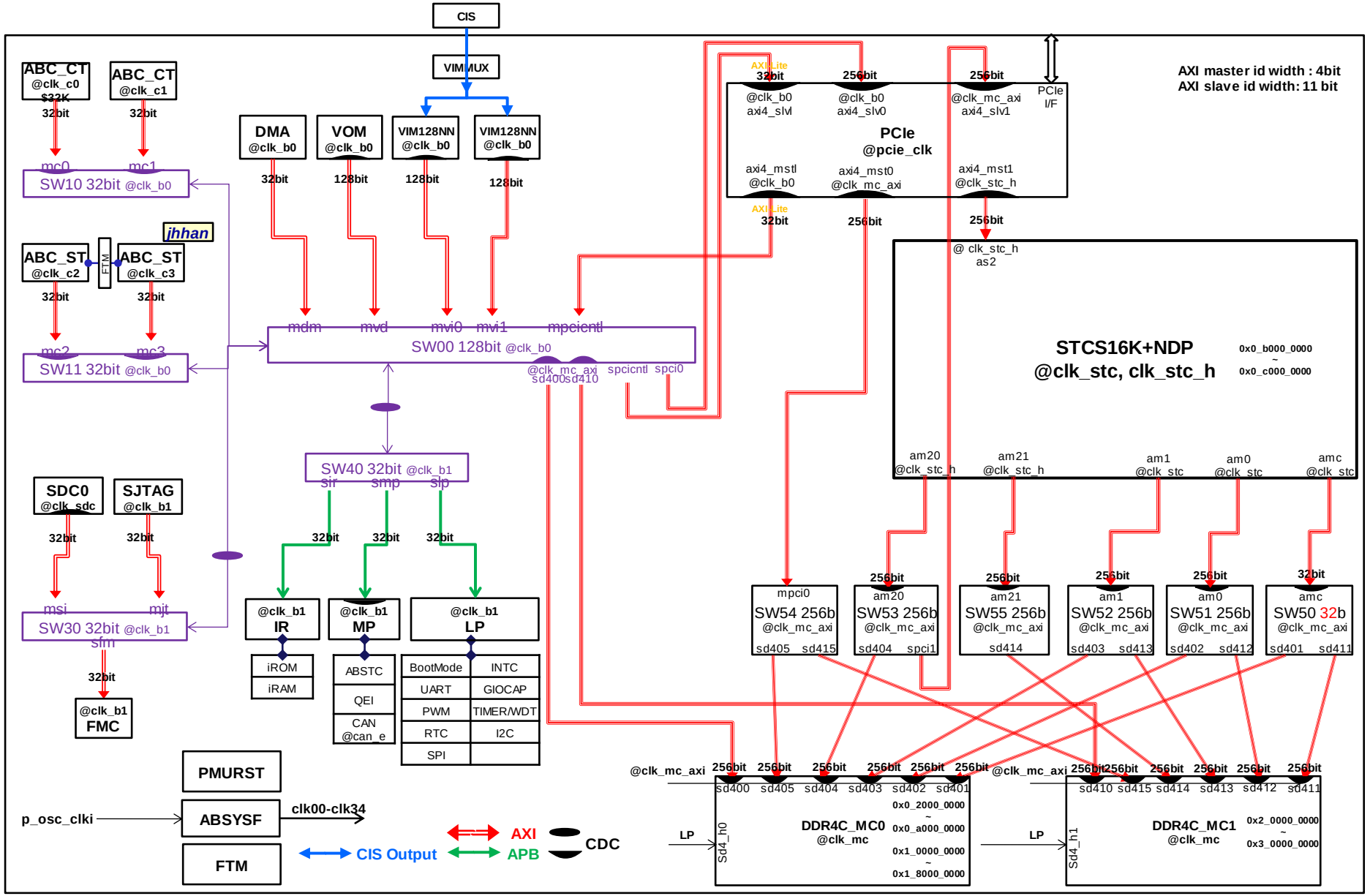
Name	AB9, 2019
Technology	28nm 1P12M Logic CMOS
Chip Size	494mm^2
Gate Count	1 Billion gates
Supply Voltage	1.05V ~ 1.15V
Clock Frequency	600MHz ~ 1.2GHz
AI Performance	32TFLOPS
GP Processor Core	2 x 1GHz Processor Core 2 x 1GHz Function-safe Core
AI Processor Core	128 x 128 1GHz Nano Cores
Feature/Kernel Memory	40MB 1GHz SRAM (+8MB Redundancy)
External Memory Interface	2 x LPDDR4 Controller
External Interface	16-Lane PCIE Gen3
AI SDE	Neural Net Compiler, Simulator

AI Software Development Environment

- STC CMD Compiler, STC Simulator, Device Driver API for GPP
- Input: NN_DESC, HW_DESC, NN_WEIGHT
- Output: STC Command, All Layer Top Code, Simulator Top

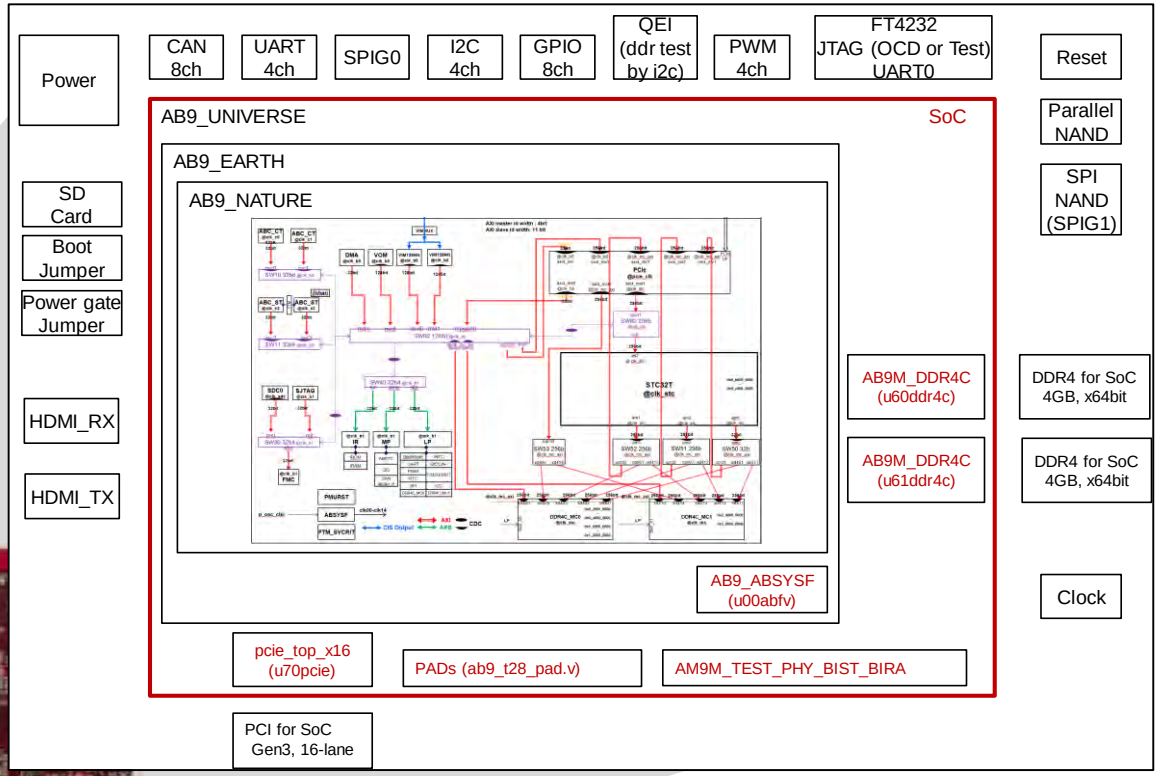


AB9: Artificial Intelligence Processor

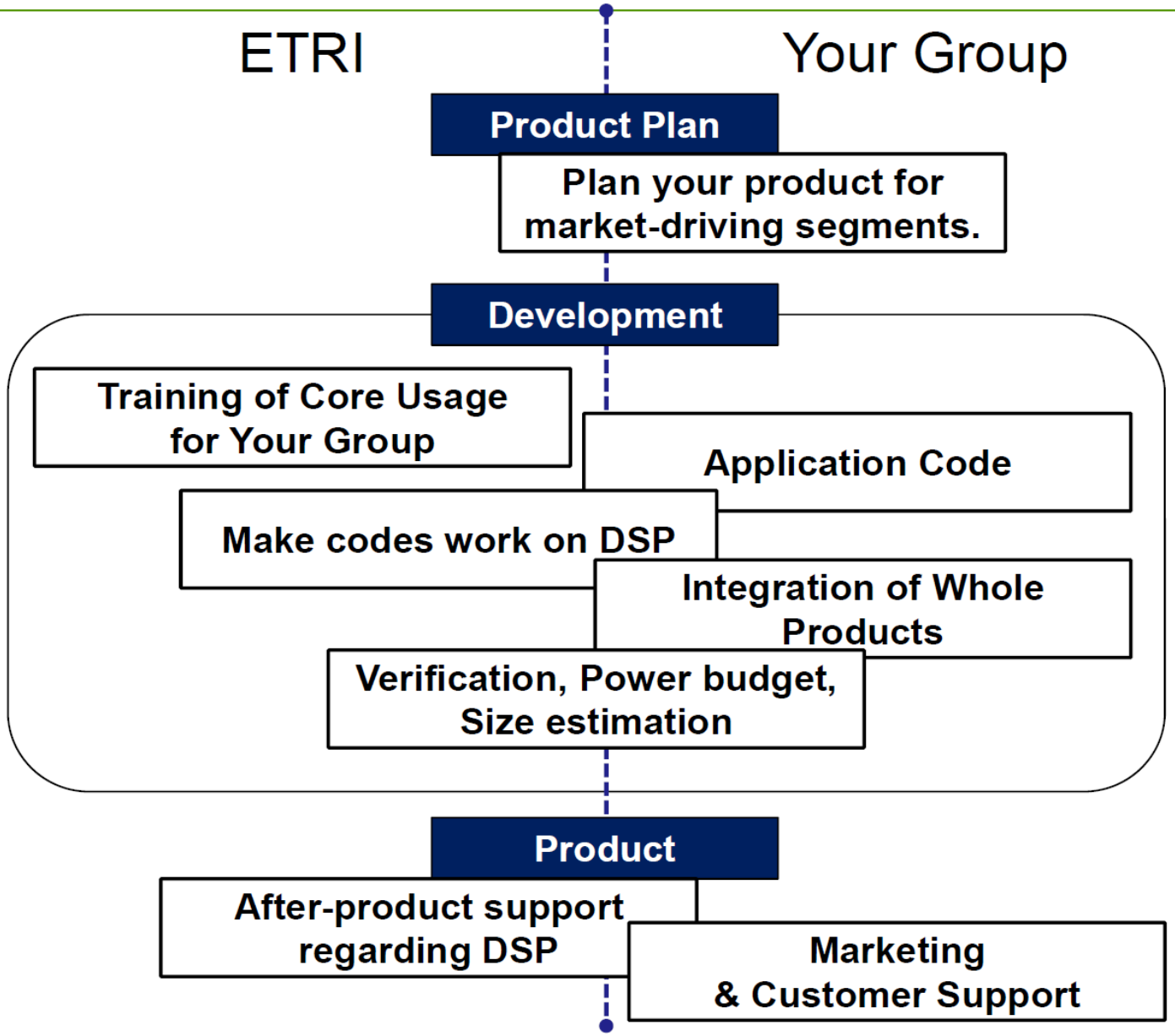


FPGA Board

- Xilinx Vertex Ultrascale 440(5,541 K Logic, 88.6Mb), 16x128 w/ 4MB
- JTAG Interface for On-chip debugging and Probing
- 2 x 4GB DDR4, 8-lane PCIE Gen3



Co-Development with ETRI



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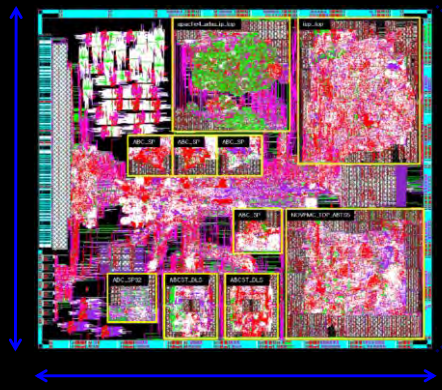
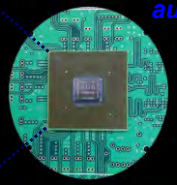




Aldebaran is a high-performance, low-power ANN processor platform with functional safety for large-scale server applications as well as autonomous driving.

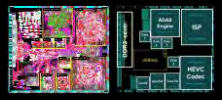
AB9, ANN 32T Processor

Many-Core ANN 16384x Processor
32Tera-FLOPS Super-Thread Core
16384 1.0GHz Neural Core@28nm
Multi-Chip Scalable Processors
AI Server/Server Computing Module

AB11, ANN 8T Processor

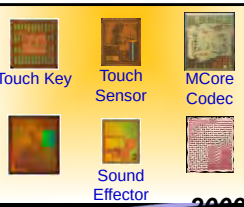
Many-Core ANN 4096x Processor
8Tera-FLOPS Super-Thread Core
4096 1.0GHz Neural Core@28nm
Autonomous Driving AI Processor

Nona-Core (9x)
1.2GHz@28nm
9x Superscalar Cores
ISO 26262 ASIL-D Compliance
Autonomous Driving Safety
Dynamic Lockstep
Self-recovering Cache
HEVC 4K/4K Codec Engine
VD/PD/LD/MOD Engine
Image Signal Processor

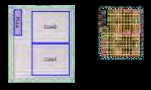


AB-EMP, MCU DSP

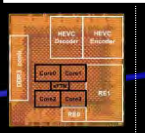
Dual/Quad-Core/Multi-Port SPM
160 instructions
500MOPS@130nm
35Kgates, 3mW/core@130nm



Dual-Core (2x)
800MHz@65nm
ETRI 32b Processor Architecture
Superscalar 32-bit
Low-Power Dynamic V-F Scaling
32K L1 I/D Cache
Virtual Memory MMU



Quad-Core (4x)
1.0GHz@28nm
LINUX/RTEMS/AUTOSAR OS
HEVC 4K/2K Codec
CAN(8x), DSP
Recognition Engine
Functional Safety Memory



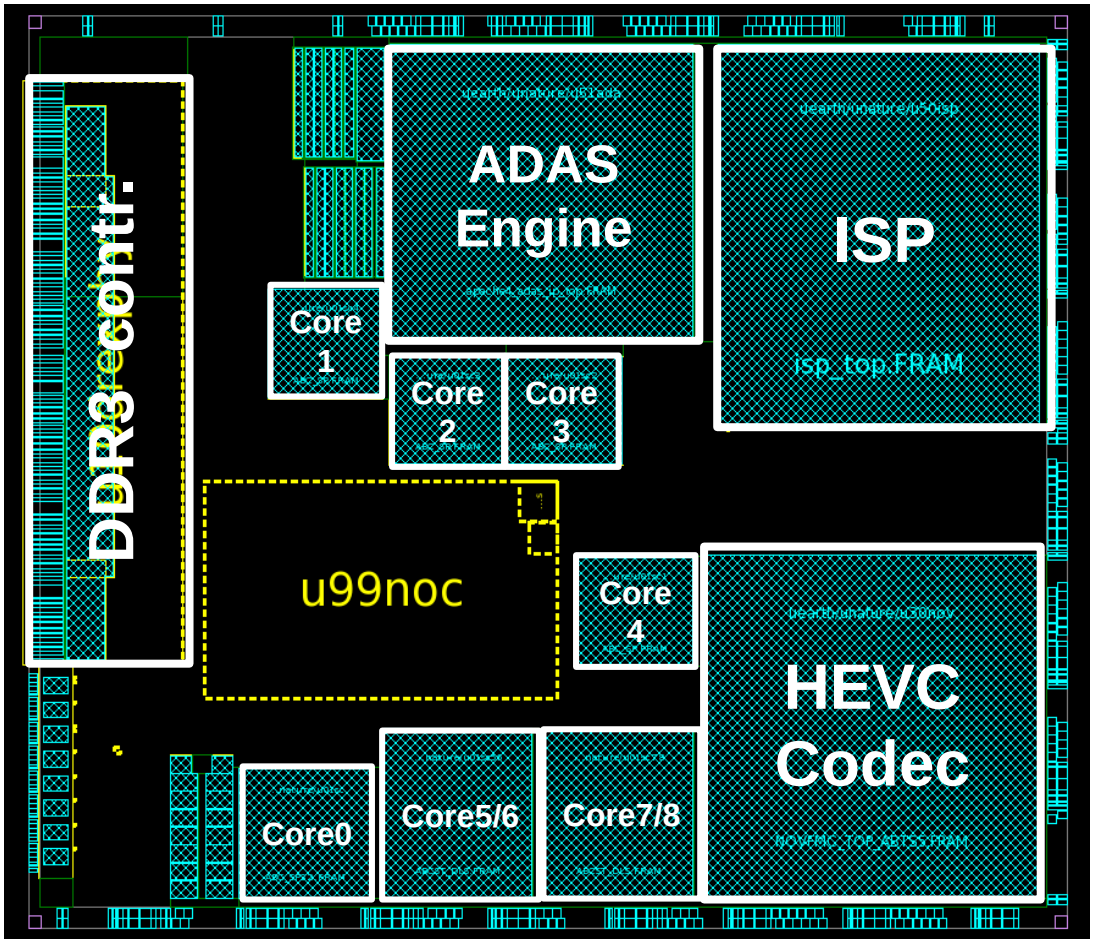
Dual-Core (2x)
Mobile Robot Processor
Dynamic Lockstep
250MHz@130nm
4x QEI, 4x CAN

AB-TN7

Single-Core
Smart Metering Processor
Superscalar core plus EMB
100MHz@180nm
SPI-G, ADC 7x22-bit Sigma-Delta

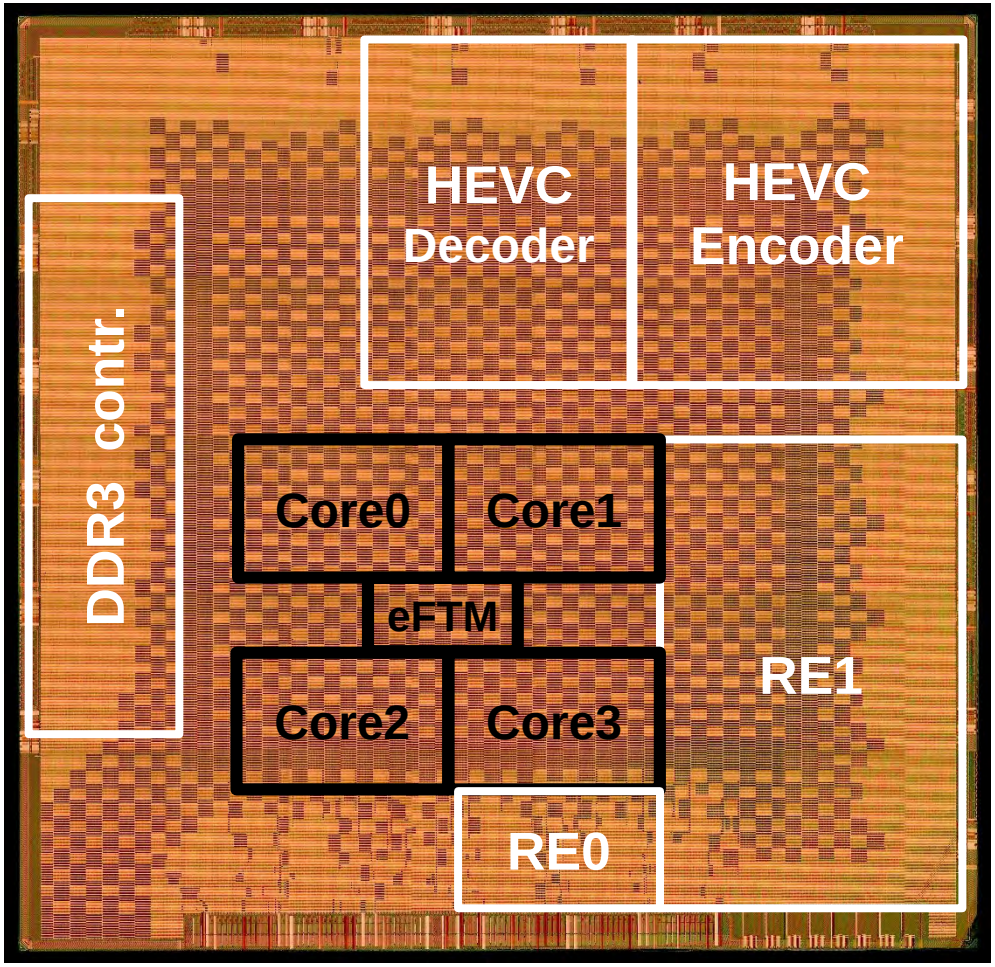
AB-TN7, 2017

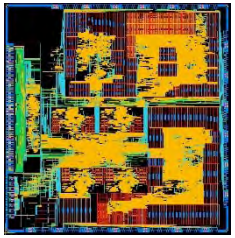
Aldebaran5



Name	AB5 (Aldebaran 5), 2017
Technology	28nm 1P12M Logic CMOS
Chip Size	7800x6700 μm^2
Gate Count With SRAM	33M gates
Supply Voltage	1.05V ~ 1.15V
Clock Frequency	600MHz ~ 1.0GHz
Core 0 Gate Count	524K gates
Core 1 Gate Count	463K gates
Core 5/6 Gate Count	767K gates
Core Types	5 x Superscalar In-order Dual-Issue Cores 4 x Superscalar In-order Dynamic Lockstep Cores
IPs	HEVC Codec, ISP ADAS Engine 8 x CAN Controllers 4 x QEI Controllers 2 x SPI Controllers DMA Controller Video Output Controller Video Input Controller UART, I2C, SD Card
M.P.	Tech. Transfer Done. M.P. for 2017

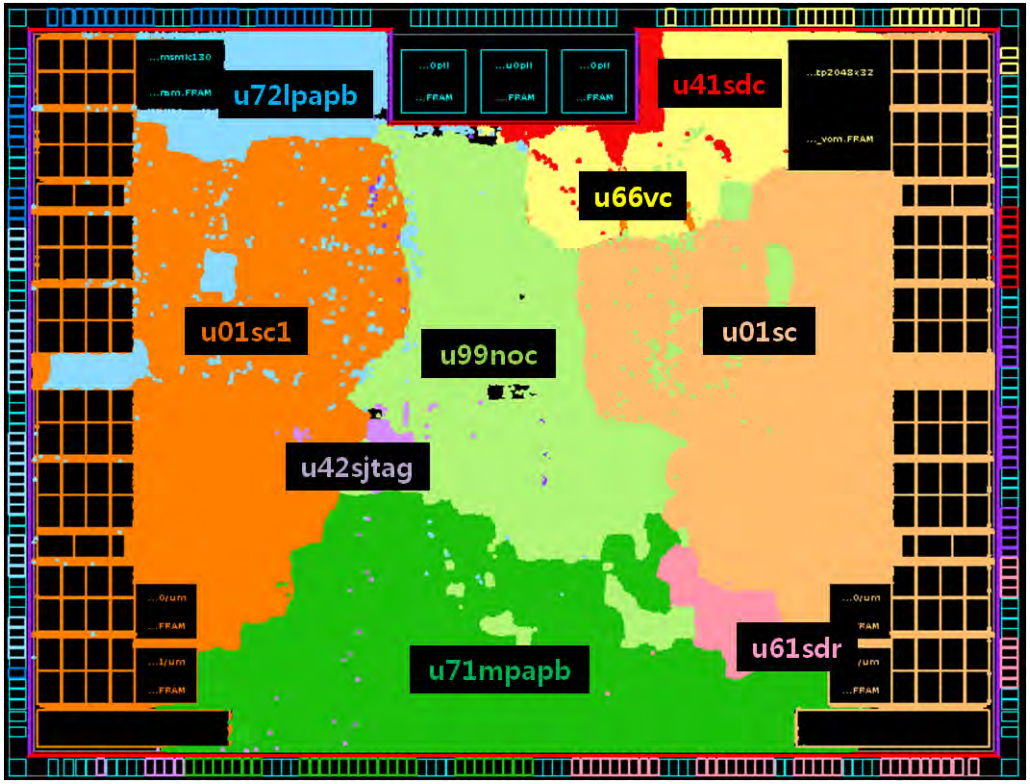
Aldebaran3





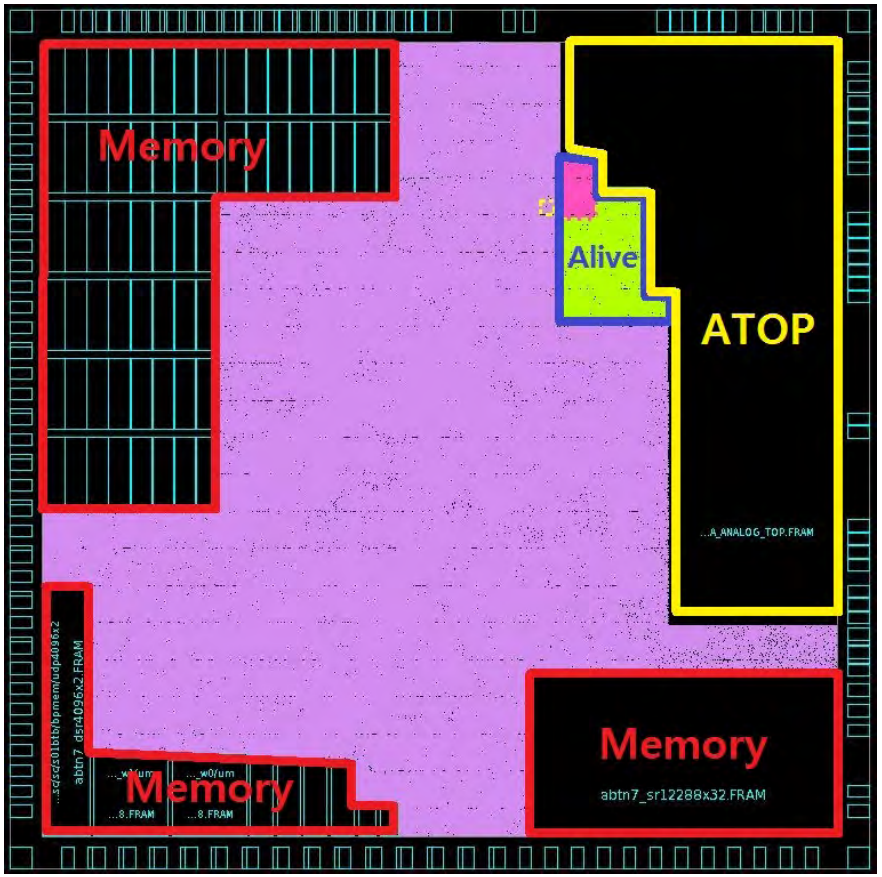
Name	AB3 (Aldebaran3), 2016
Technology	28nm 1P12M Logic CMOS
Chip Size	7341x7541 μm^2
Gate Count	18M gates
SRAM	1,077KB
Supply Voltage	1.05V ~ 1.15V
Clock Frequency	50MHz ~ 1.0GHz
Core Size	1505.8 x 1246.4 μm^2
Core Gate Count	216K gates
Core SRAM	110KB
Core #	4 Cores
IPs	HEVC Decoder HEVC Encoder Recognition Engine EMP DSP 8 x CAN Controllers DMA Controller Video Output Controller Video Input Controller UART, I2C, AC97, USB, SD Card
M.P	Tech.Transfer done. M.P. for 2017

AB-TN5



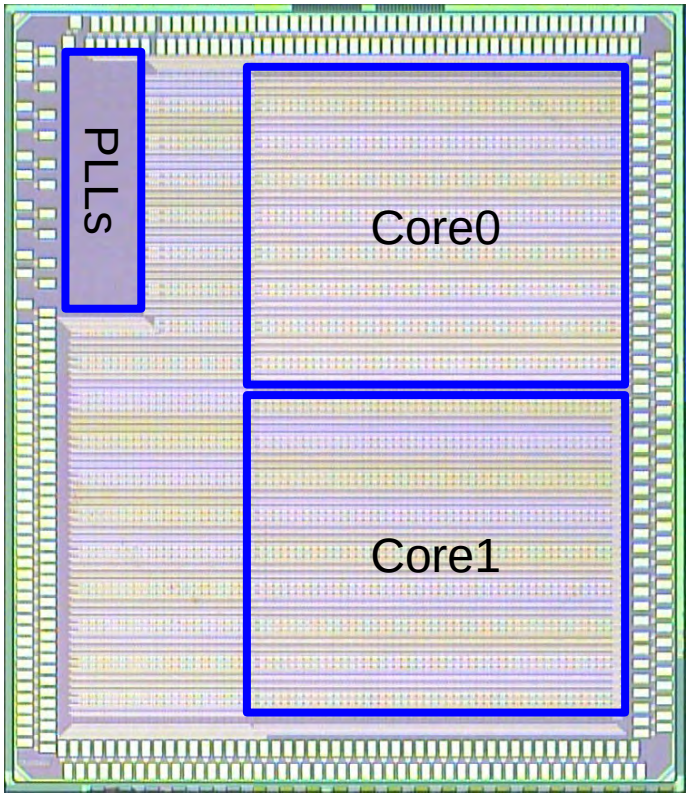
Name	AB-TN5 (Nano), 2017
Technology	130nm 1P4M Logic CMOS
Chip Size	4250x4250 μm^2
Gate Count With SRAM	4M gates
Supply Voltage	1.2V
Clock Frequency	200MHz
Core Gate Count	-
Core SRAM	-
Core Type	2 x Superscalar In-order Dynamic LockStep Cores
IPs	Timer/WDT/RTC I2C/UART/SPI FMC/SDRAM/SDC Controller 4 x QEI Controllers 4 x CAN Controllers PWM Controller GIOCAP Controller Video Output Controller
M.P.	Tech. Transfer for 2017 M.P. for 2018

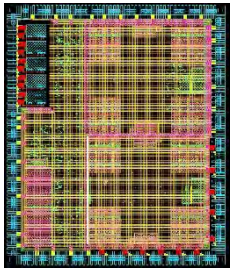
AB-TN7



Name	AB-TN7(Nano), 2017
Technology	130nm 1P4M Logic CMOS
Chip Size	4250x4250 μm^2
Gate Count With SRAM	2.3M gates
Supply Voltage	1.2V
Clock Frequency	~50MHz
Core Gate Count	-
Core SRAM	-
Core Type	Superscalar In-order Dual-Issue Core
IPs	Timer/WDT/RTC I2C/UART/USART/SPI FMC Controller SPI-G Controller for Serial NOR Flash PWM, GIOCA Sensor IF ADC(7 x 22-bit Sigma-Delta and 10-bit Aux) LCD Driver EMB Hall Sensor, Temp. Sensor Pulse Generators
M.P.	Tech. Transfer Done. M.P. for 2017

Aldebaran1





Name	AB1 (Aldebaran 1), 2014
Technology	65nm Logic CMOS
Chip Size	3000x4000 μm^2
Gate Count With SRAM	2.7M gates
Supply Voltage	1.1V
Clock Frequency	500MHz~800MHz
Core Types	Superscalar core
IPs	DVFS Manager On-Chip Bus Video Output I2C/UART/AC97/USB
M.P.	Tech. Transfer Done